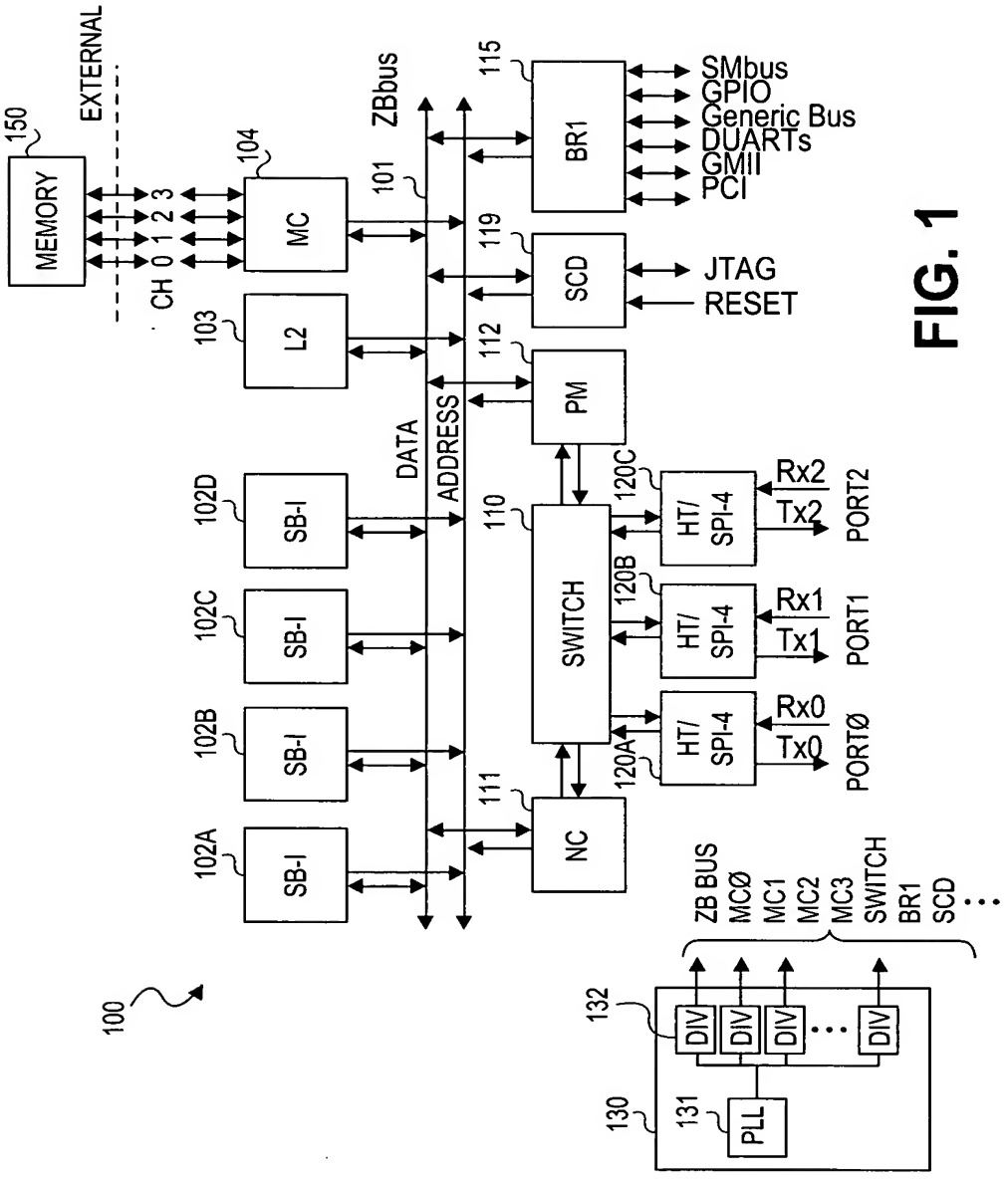
EXTERNAL
150
MEMORY
CH 0 1 2 3
104
MC
101
ZBbus
115
BR1
SMbus
GPIO
Generic Bus
DUARTs
GMII
PCI
119
SCD
JTAG
RESET
103
L2
112
PM
DATA
ADDRESS
102D
SB-I
102C
SB-I
102B
SB-I
102A
SB-I
110
SWITCH
111
NC
120C
HT/
SPI-4
Rx2
Tx2
PORT2
120B
HT/
SPI-4
Rx1
Tx1
PORT1
120A
HT/
SPI-4
Rx0
Tx0
PORTØ
ZB BUS
MCØ
MC1
MC2
MC3
SWITCH
BR1
SCD
132
DIV
DIV
DIV
DIV
130
131
PLL
100

FIG. 1

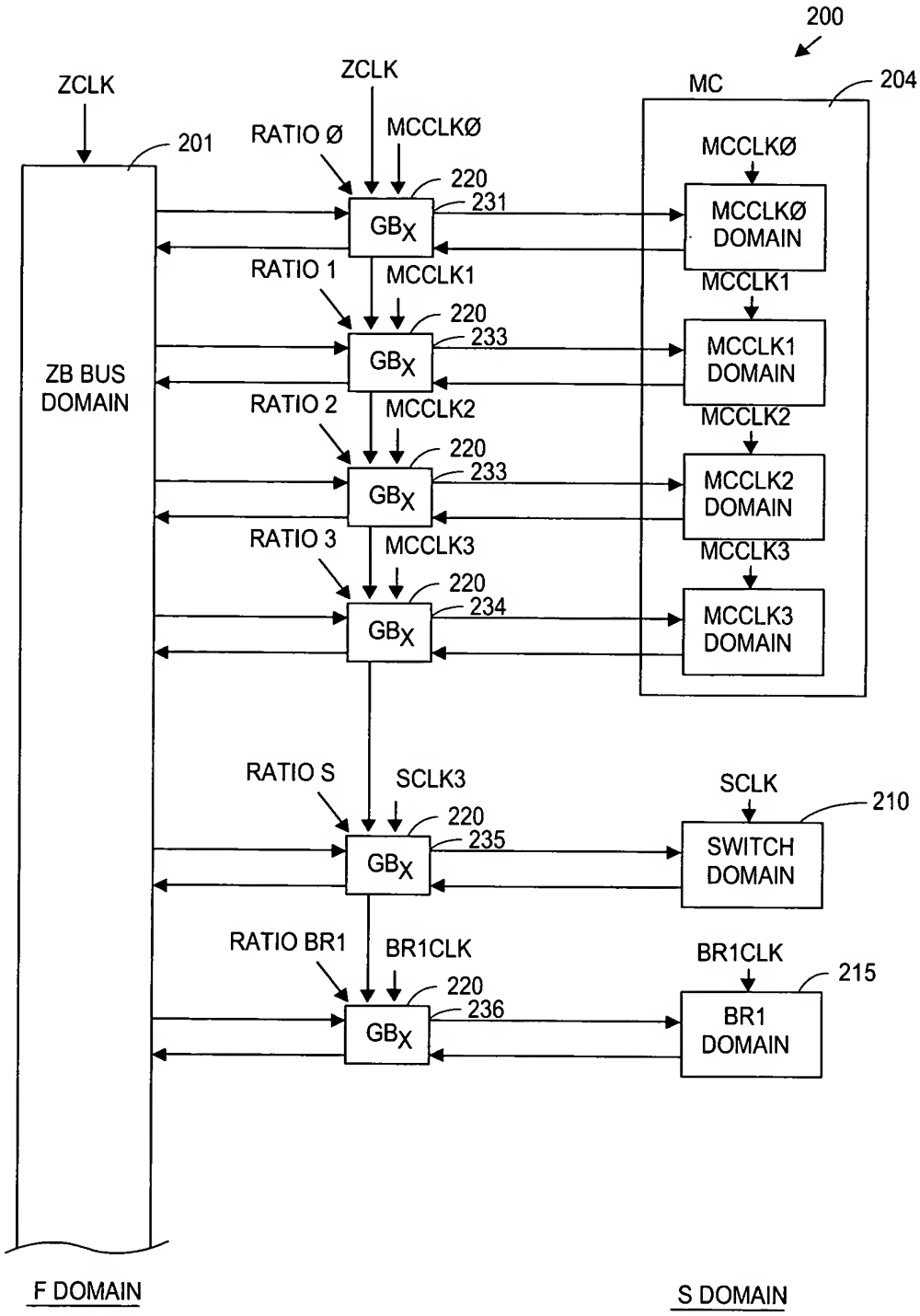
200
ZCLK
ZCLK
MC
204
201
RATIO Ø
MCCLKØ
MCCLKØ
220
231
GBX
MCCLKØ DOMAIN
RATIO 1
MCCLK1
MCCLK1
220
233
GBX
MCCLK1 DOMAIN
ZB BUS DOMAIN
RATIO 2
MCCLK2
MCCLK2
220
233
GBX
MCCLK2 DOMAIN
RATIO 3
MCCLK3
MCCLK3
220
234
GBX
MCCLK3 DOMAIN
RATIO S
SCLK3
SCLK
210
220
235
GBX
SWITCH DOMAIN
RATIO BR1
BR1CLK
BR1CLK
215
220
236
GBX
BR1 DOMAIN
F DOMAIN
S DOMAIN

FIG. 2

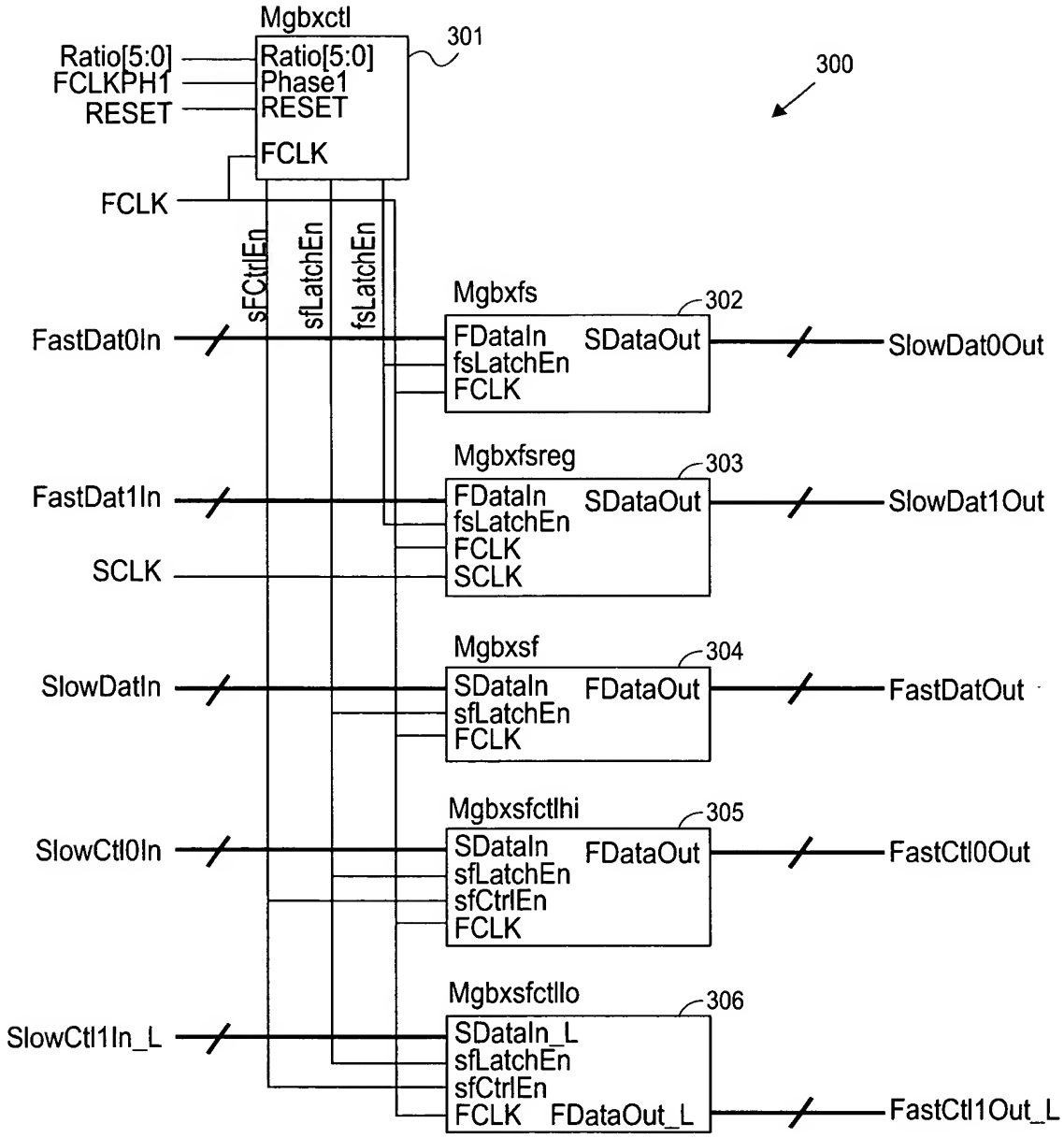
Mgbxctl
301
Ratio[5:0]
FCLKPH1
RESET
Ratio[5:0]
Phase1
RESET
FCLK
FCLK
300
sECtrlEn
sfLatchEn
fsLatchEn
Mgbxfs
302
FastDat0In
FDataIn
fsLatchEn
FCLK
SDataOut
SlowDat0Out
Mgbxfsreg
303
FastDat1In
SCLK
FDataIn
fsLatchEn
FCLK
SCLK
SDataOut
SlowDat1Out
Mgbxsf
304
SlowDatIn
SDataIn
sfLatchEn
FCLK
FDataOut
FastDatOut
Mgbxsfctlhi
305
SlowCtl0In
SDataIn
sfLatchEn
sfCtrlEn
FCLK
FDataOut
FastCtl0Out
Mgbxsfctllo
306
SlowCtl1In_L
SDataIn_L
sfLatchEn
sfCtrlEn
FCLK
FDataOut_L
FastCtl1Out_L

FIG. 3

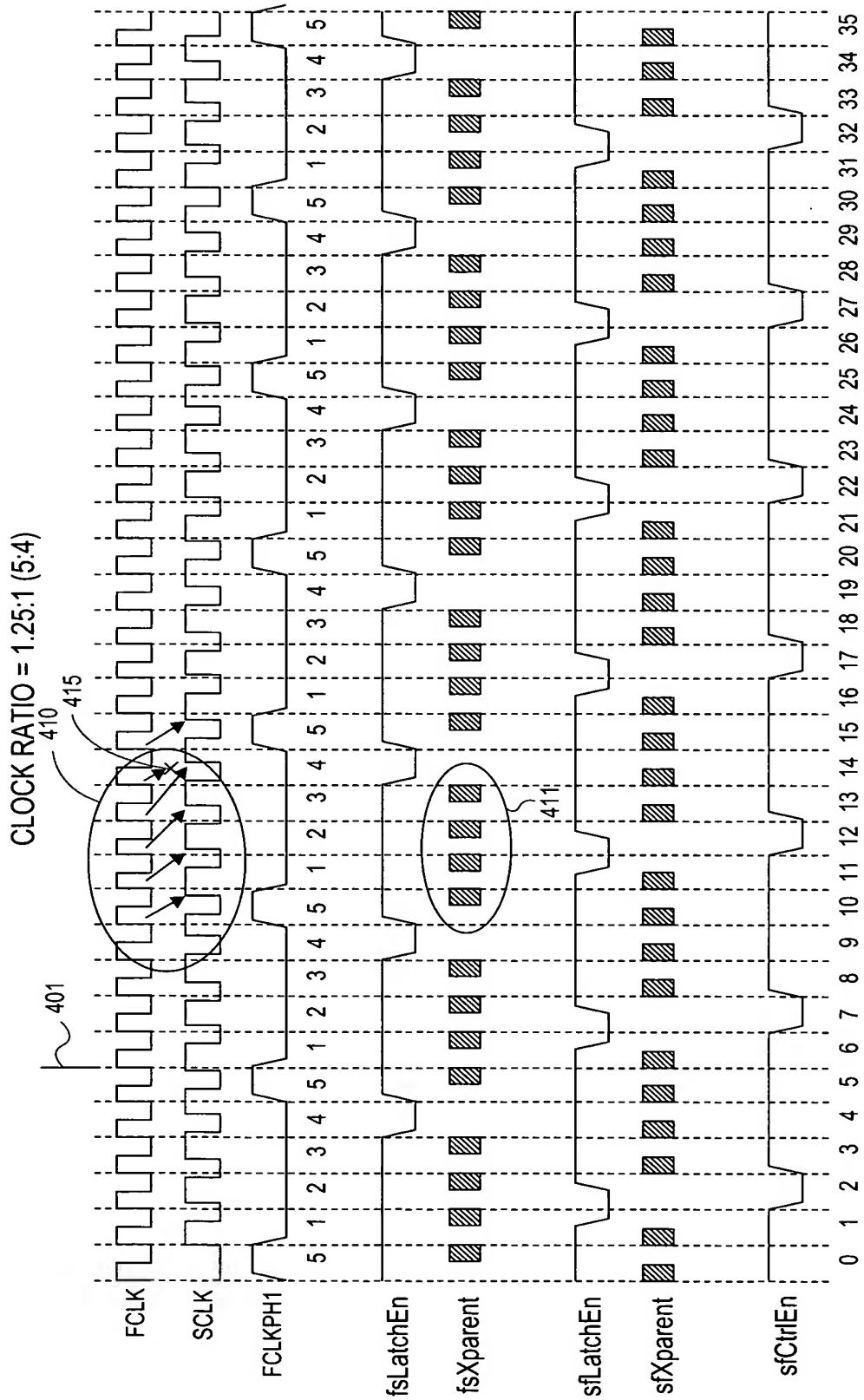
CLOCK RATIO = 1.25:1 (5:4)
401
410
415
411
FCLK
SCLK
FCLKPH1
fsLatchEn
fsXparent
sfLatchEn
sfXparent
sfCtrlEn
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35

FIG. 4

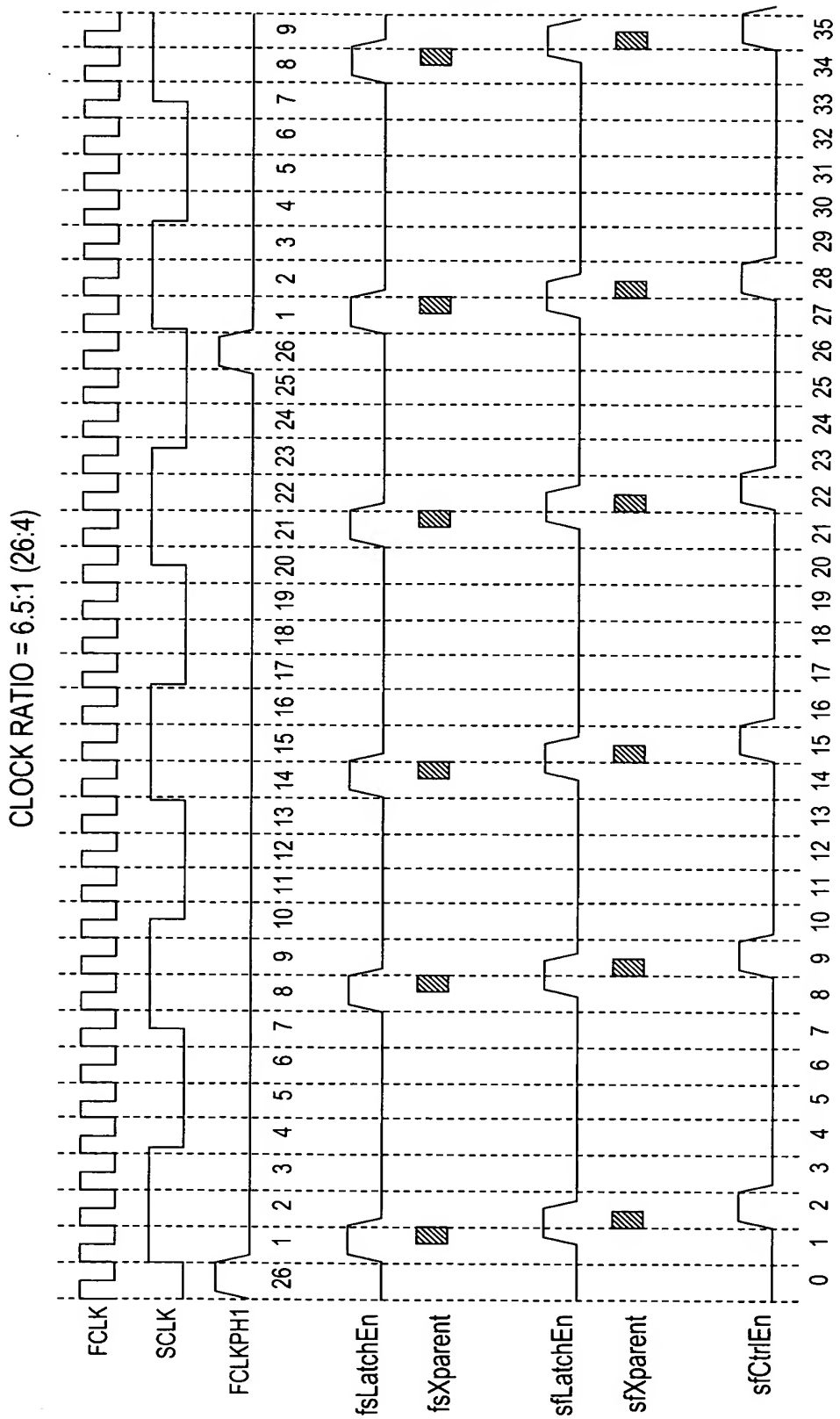
CLOCK RATIO = 6.5:1 (26:4)
FCLK
SCLK
FCLKPH1
fsLatchEn
fsXparent
sfLatchEn
sfXparent
sfCtrlEn
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
26 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 1 2 3 4 5 6 7 8 9

FIG. 5

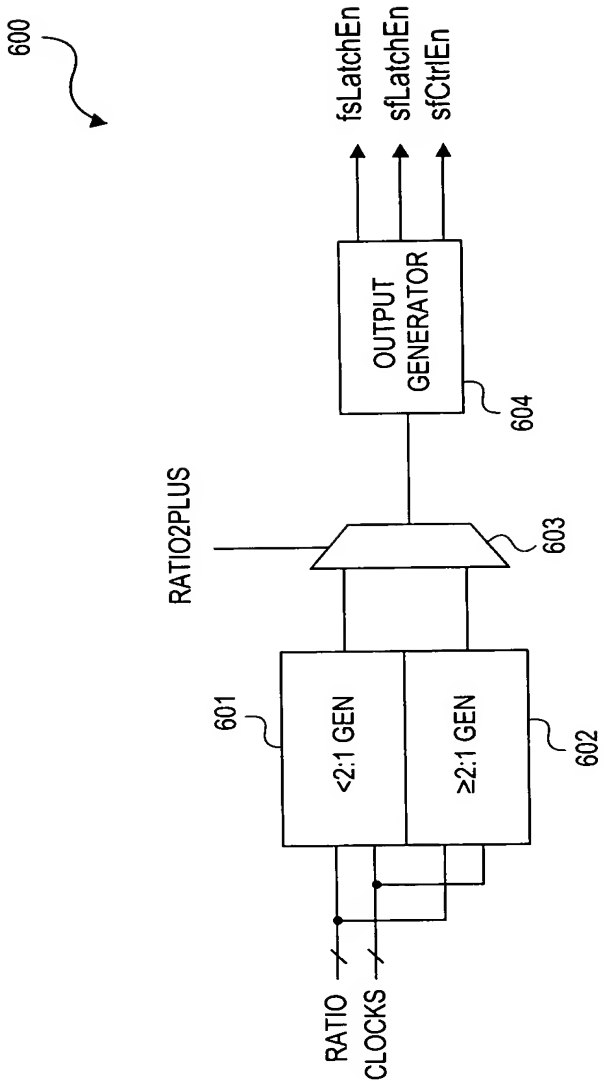
600
fsLatchEn
sfLatchEn
sfCtrlEn
OUTPUT GENERATOR
604
RATIO2PLUS
603
601
<2:1 GEN
≥2:1 GEN
602
RATIO
CLOCKS

FIG. 6

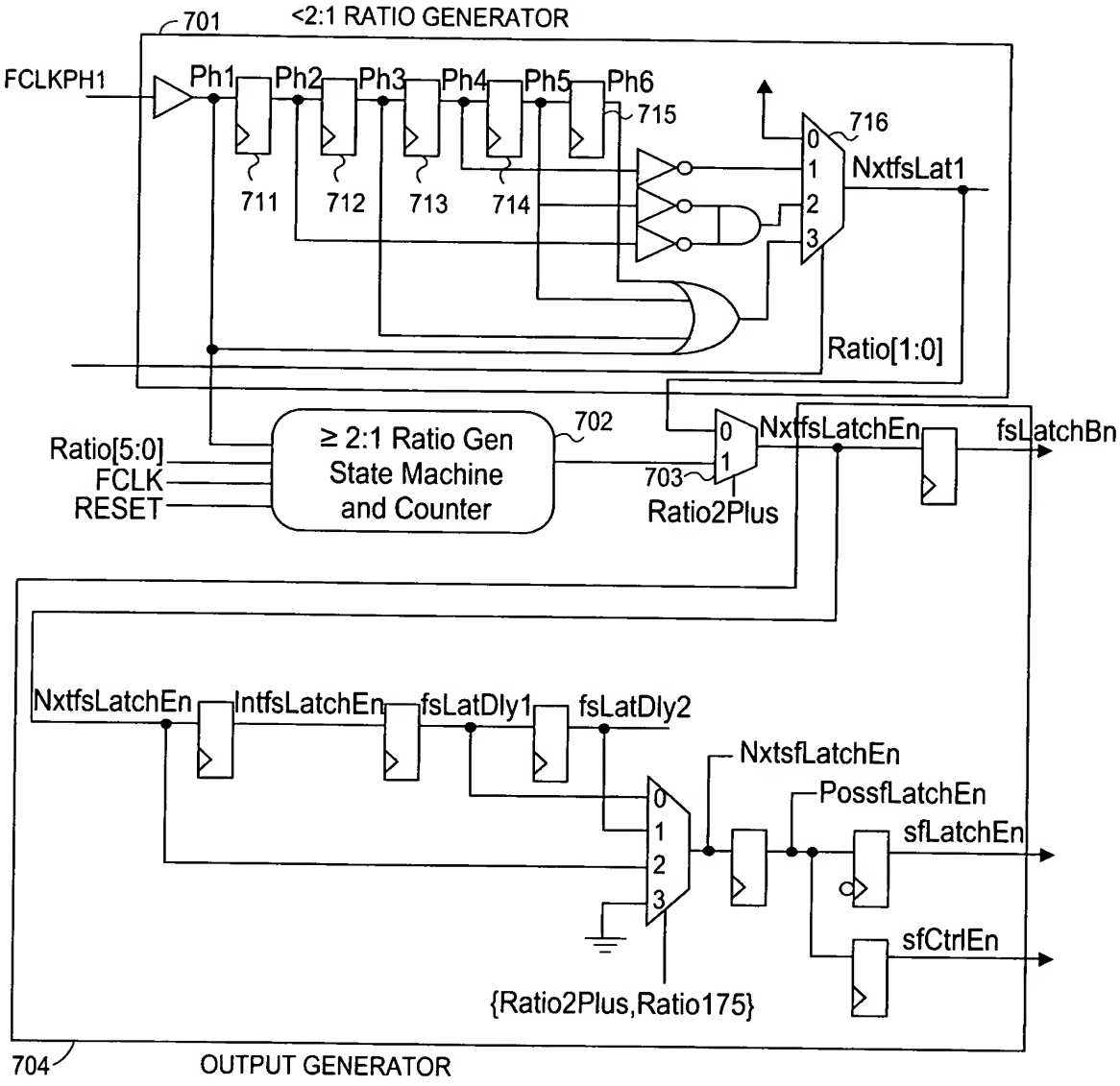
701
<2:1 RATIO GENERATOR
FCLKPH1
Ph1
Ph2
Ph3
Ph4
Ph5
Ph6
715
716
711
712
713
714
0
1
2
3
NxtfsLat1
Ratio[1:0]
Ratio[5:0]
FCLK
RESET
≥ 2:1 Ratio Gen
State Machine
and Counter
702
703
Ratio2Plus
NxtfsLatchEn
fsLatchBn
NxtfsLatchEn
IntfsLatchEn
fsLatDly1
fsLatDly2
NxtsfLatchEn
PossfLatchEn
sfLatchEn
sfCtrlEn
{Ratio2Plus,Ratio175}
704
OUTPUT GENERATOR

FIG. 7

fsLatchEn Generation for Clock Ratios Below 2:1

Ratio[5:0]	Clock Ratio	Behavior
4	1.00:1	fsLatchEn always asserted.
5	1.25:1	fsLatchEn asserted in all FCLKs except Phase 5.
6	1.50:1	fsLatchEn asserted in all FCLKs except Phases 3 and 6.
7	1.75:1	fsLatchEn asserted in Phases 2, 4, 6 and 7.

FIG. 8

sfLatchEn Generation as a Function of Clock Ratio

Clock Ratio	Behavior
1.00:1	Don't Care. Implemented as a 2.5 FCLK delay from fsLatchEn.
1.25:1	sfLatchEn is delayed 2.5 FCLKs from fsLatchEn.
1.50:1	sfLatchEn is delayed 2.5 FCLKs from fsLatchEn.
1.75:1	sfLatchEn is delayed 3.5 FCLKs from fsLatchEn.
2.00:1 and up	sfLatchEn is delayed 0.5 FCLKs from fsLatchEn.

FIG. 10

fsLatchEn Generation for Clock Ratios 2:1 and Above

Ratio[5:0]	Clock Ratio	Behavior
8	2.00:1	fsLatchEn asserts in a 2-2-2-2 pattern. That is, a repeating 1-0-1-0-1-0-1-0 pattern for a total of 9 FCLKs.
9	2.25:1	fsLatchEn asserts in a 3-2-2-2 pattern. That is, a repeating 1-0-0-1-0-1-0-1-0 pattern for a total of 9 FCLKs.
10	2.50:1	fsLatchEn asserts in a 3-2-3-2 pattern.
11	2.75:1	fsLatchEn asserts in a 3-3-3-2 pattern.
12	3.00:1	fsLatchEn asserts in a 3-3-3-3 pattern.
13	3.25:1	fsLatchEn asserts in a 4-3-3-3 pattern.
14	3.50:1	fsLatchEn asserts in a 4-3-4-3 pattern.
15	3.75:1	fsLatchEn asserts in a 4-4-4-3 pattern.
16	4.00:1	fsLatchEn asserts in a 4-4-4-4 pattern.
17	4.25:1	fsLatchEn asserts in a 5-4-4-4 pattern.
18	4.50:1	fsLatchEn asserts in a 5-4-5-4 pattern.
19	4.75:1	fsLatchEn asserts in a 5-5-5-4 pattern.
20	5.00:1	fsLatchEn asserts in a 5-5-5-5 pattern.
21	5.25:1	fsLatchEn asserts in a 6-5-5-5 pattern.
22	5.50:1	fsLatchEn asserts in a 6-5-6-5 pattern.
23	5.75:1	fsLatchEn asserts in a 6-6-6-5 pattern.
24	6.00:1	fsLatchEn asserts in a 6-6-6-6 pattern.
25	6.25:1	fsLatchEn asserts in a 7-6-6-6 pattern.
26	6.50:1	fsLatchEn asserts in a 7-6-7-6 pattern.
27	6.75:1	fsLatchEn asserts in a 7-7-7-6 pattern.
28	7.00:1	fsLatchEn asserts in a 7-7-7-7 pattern.
29	7.25:1	fsLatchEn asserts in a 8-7-7-7 pattern.
30	7.50:1	fsLatchEn asserts in a 8-7-8-7 pattern.
31	7.75:1	fsLatchEn asserts in a 8-8-8-7 pattern.
32	8.00:1	fsLatchEn asserts in a 8-8-8-8 pattern.

FIG. 9

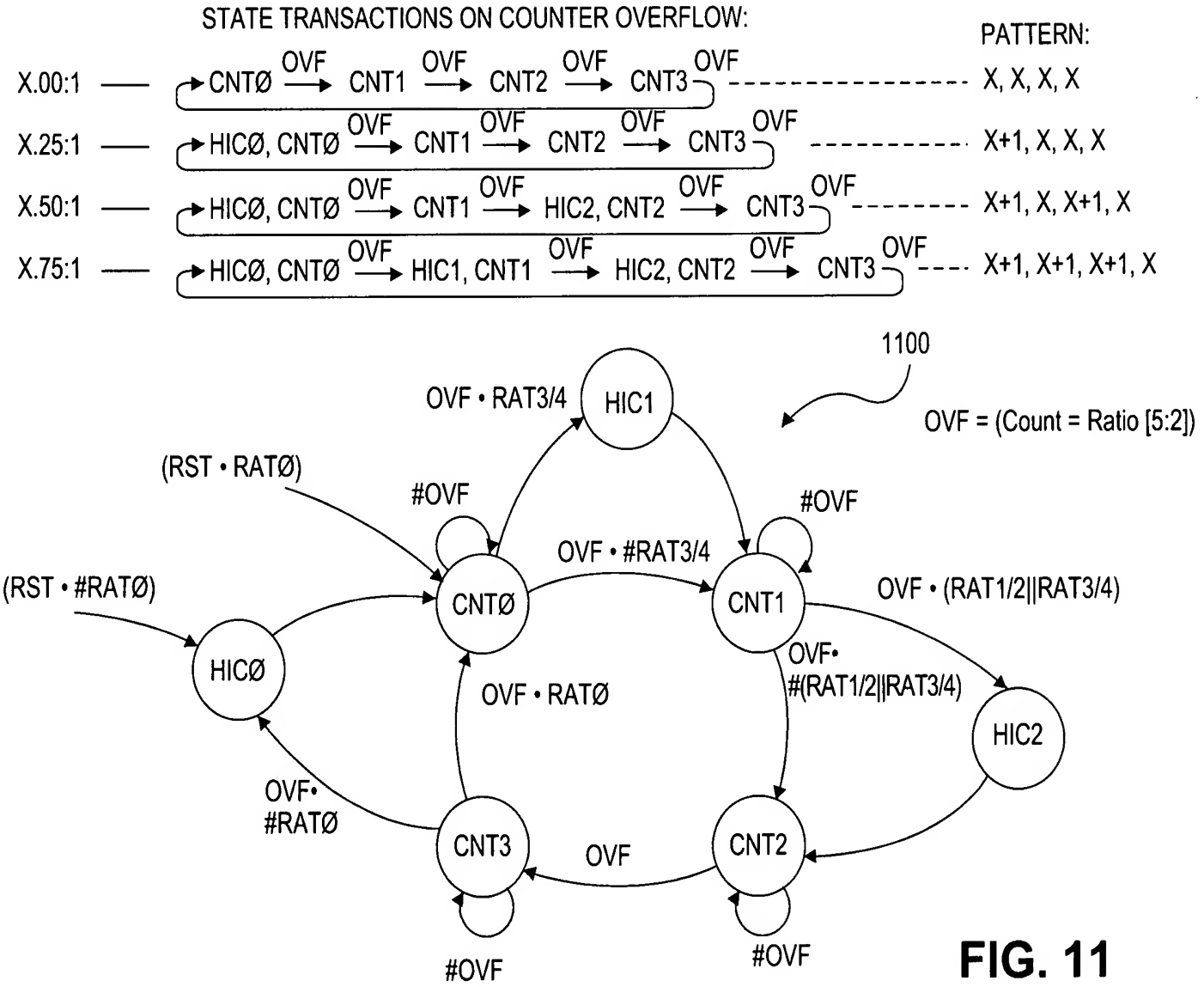
STATE TRANSACTIONS ON COUNTER OVERFLOW:
PATTERN:
X.00:1
CNTØ
OVF
CNT1
OVF
CNT2
OVF
CNT3
OVF
X, X, X, X
X.25:1
HICØ, CNTØ
OVF
CNT1
OVF
CNT2
OVF
CNT3
OVF
X+1, X, X, X
X.50:1
HICØ, CNTØ
OVF
CNT1
OVF
HIC2, CNT2
OVF
CNT3
OVF
X+1, X, X+1, X
X.75:1
HICØ, CNTØ
OVF
HIC1, CNT1
OVF
HIC2, CNT2
OVF
CNT3
OVF
X+1, X+1, X+1, X
1100
OVF = (Count = Ratio [5:2])
HIC1
OVF • RAT3/4
(RST • RATØ)
#OVF
#OVF
OVF • #RAT3/4
(RST • #RATØ)
CNTØ
CNT1
OVF • (RAT1/2||RAT3/4)
HICØ
OVF•
#(RAT1/2||RAT3/4)
OVF • RATØ
HIC2
OVF•
#RATØ
CNT3
OVF
CNT2
#OVF
#OVF

FIG. 11

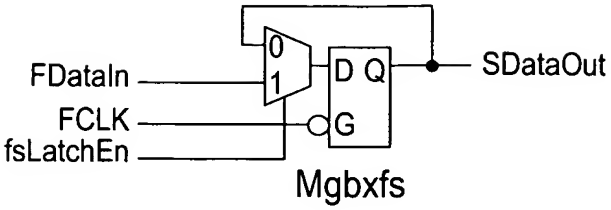

FIG. 12

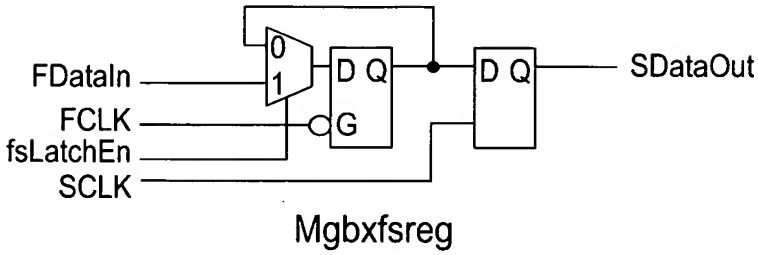

FIG. 13

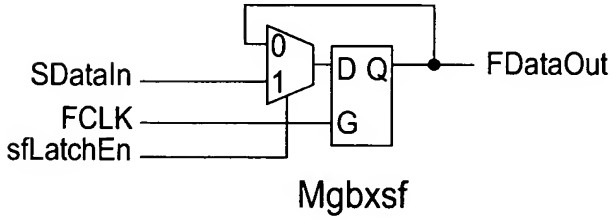

FIG. 14

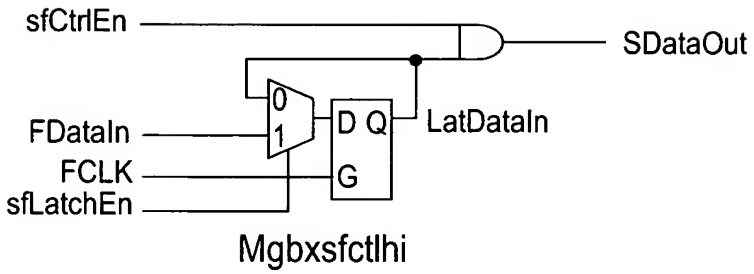
sfCtrlEn
SDataOut
0
1
D Q
LatDataIn
FDataIn
FCLK
G
sfLatchEn
Mgbxsfctlhi

FIG. 15

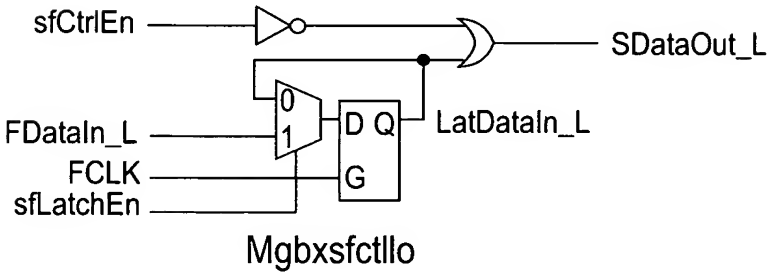
sfCtrlEn
SDataOut_L
0
1
D Q
LatDataIn_L
FDataIn_L
FCLK
G
sfLatchEn
Mgbxsfctllo

FIG. 16